800

FIG. 8A (Amended)

(Prior Art)

entity Fsm: Fsm

850

800

Fsm_state(01..2)

801

Fsm_clock
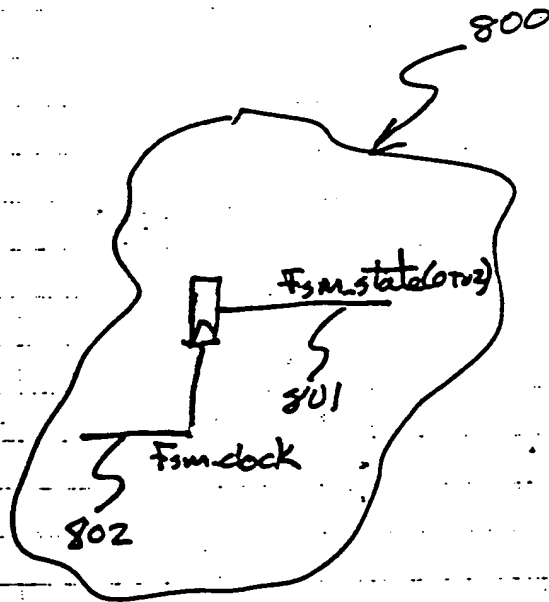
802

FIG. 8B (Amended)

(Prior Art)

```
entity Fsm IS ●                    ●
  PORT (
          .... ports for entity Fsm.....
      );

ARCHITECTURE Fsm of Fsm IS

  BEGIN

      .... HDL code For Fsm and rest of the entity...

      Fsm_state(0 to 2) <= ... signal 801.---

853{    --!! Embedded Fsm : exampleFsm;
859{    --!! clock         :(fsm_clock);
854{    --!! state_vector   :(Fsm-state(0 to 2));
855{    --!! states         :(s0, s1, s2, s3, s4);
856{    --!! state_encoding :('000', '001', '000', '011', '100');
857[    --!! arcs           :(s0=>s0, s0=>s1, s0=>s2,
        --!!                  s1=>s2, s1=>s3, s2=>s2,
        --!!                  s2=>s3, s3=>s4, s4=>s0);
858{    --.! end Fsm;
```



```
  END;
```

FIG. 8C (Amended)